ABSTRACT

A programmed Flash EPROM memory cell has a charge stored on a floating gate located between the control gate and the channel of a MOS device. To erase the memory cell, the source voltage (V_S) is set to a positive voltage and the control gate voltage (V_{CG}) is set to a negative voltage while the drain floats. An electric field forms between the source and floating gate removing the negative charge on the floating gate. The minimum required erase voltage increases with the number of program and erasure cycles performed. In order to predict the function of the device over the devices lifetime, a lower voltage is typically used during chip probe testing. This lower voltage test is referred to as marginal erase. If the memory will erase at this lower voltage at wafer probe, then it is statistically predicted. The present invention describes a method whereby margin erase testing is achieved by using a method where series connected voltage-dropping components are bypassed to the point of application of the erase voltage (V_E). During testing, these bypassed components reduce the voltage applied to the memory cell to the margin erase voltage level. If a plurality of diode-connected NMOS transistors are used as the voltage dropping components, the voltage applied to the memory cell array is reduced by $(n*V_t)$ where n is the number of bypassed diode connected NMOS transistors and V_t is the threshold voltage of the NMOS transistors. In normal operation, the voltage dropping components are not bypassed, thereby returning the voltage applied to the normal level. This method has the advantage over prior method in that the margin erase voltage tracks normal erase voltage over process variation and that no additional test bond pad is required.